PB/80 Computer

Introduction

The PB/80 is a ½ micro-second, 8 bit computer. The large instruction set, 52 instructions, and 4 general purpose registers allow efficient machine coding.

The PB/80 consists of a set of functional modules implemented with entirely TTL integrated circuitry, and a random-access memory incorporating the present state-of-the-art MOS technology.

All data transfers and manipulations within the computer are controlled by a solid state TTL LSI, read-only memory (ROM) controller. Data transfers and processing are controlled by the execution of a 12 bit set of micro-instructions stored in the ROM. A new micro-instruction is accessed and executed every 500nano-seconds. This rate allows most instructions to be accessed from memory and executed in 2 micro-seconds.

Machine Characteristics

The basic organisation of the PB/80 Computer is presented in block diagram form in figures 1-1 and 2-1. The computer consists of storage, processing and operator input/output units. All major system units are connected to the output bus (OBUS), which is the 8 bit parallel path used for all data transfers within the computer bus structure.

MEMORY
- 256 X 8 bit words (bytes).
- 450 nano-second access time.
- All memory locations directly addressable.

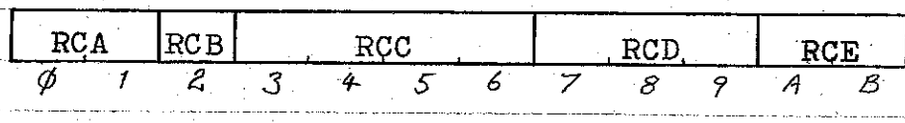
GENERAL PURPOSE REGISTER FILE
- 4 addressable, 8 bit general purpose registers.
- 3 of the registers usable as index registers.
- 1½ micro-second execution time for register to register instructions.

ARITHMETIC/LOGIC UNIT
- Parallel operation.
- Full set of arithmetic, logical and shift capabilities.
- Implemented with three TTL MSI IC's.

INSTRUCTION CONTROL
- Implemented by a micro-instruction sequence by ROM control system.
- Micro-instruction word containing five basic fields.
- Codes serve to route data transfers between functional units which perform data processing.

CONTROL WORD STRUCTURE

Bit(s)	Control field.
Ø,1	RCA 'A' source
2	RCB 'B' source
3-6	RCC Arithmetic/Logic Unit
7-9	RCD Destination
A,B	RCE End (instruction finish)



Bus Structure

Units

ABM 'A' Bus Multiplex
ALU Arithmetic/Logic Unit

FPR Front Panel Register
GPR General Purpose Registers
IRR Instruction Register
MAR Memory Address Register
MEM Memory (256 X 8)
MDR Memory Data Register
PCR Programme Counter Register
TRA 'A' Bus Temporary Register

Buses

ABUS ALU 'A' input Bus
ADDR Memory address bus
BBUS ALU 'B' input bus
DATA Memory data bus
FPIB Front Panel data input bus
IRRB Instruction register bus
OBUS ALU output bus
~~PCRB~~ Programme Counter register bus
~~TRAB~~ 'A' bus temporary register bus

Sections

1-2 ALU & GPR
1-3 ~~ABM~~, PCR, FPR & TRA
1-4 MAR, MDR, MEM & IRR

Rev 'A' Delete PCRB
TRAB
ABM

Control lines

'A' Source	ABM-A ABM-B	} ABM 'A' Source select
'B' Source	GPR-RA GPR-RB	} GPR register read select
Arithmetic/ Logic Unit	ALU-M ALU-C ALU-SØ ALU-S1 ALU-S2 ALU-S3 ALU-S/N ALU-R/S ALU-L/R	} ALU function control
Destination	GPR-GW	— GPR write strobe
	GPR-WA GPR-WB	} GPR register write select
	FPR-WC PCR-WC TRA-WC MAR-WC MDR-WC IRR-WC	} Write clocks.
	MEM-R/W	— Memory read/write control
Others	ALU-CLK	— ALU data output strobe
	ZERON	— OBUS zero detect
	ZABUS	Zero ABUS

Devices

2 off 74181
1 off 74182
1 off 74198
4 off 74LS153
6 off 74LS374
2 off 74LS670
1 off 81LS95
1 off 81LS96
2 off 2112
1 off 74LS30
2 off and gates
2 off nand gates
1 off inverter

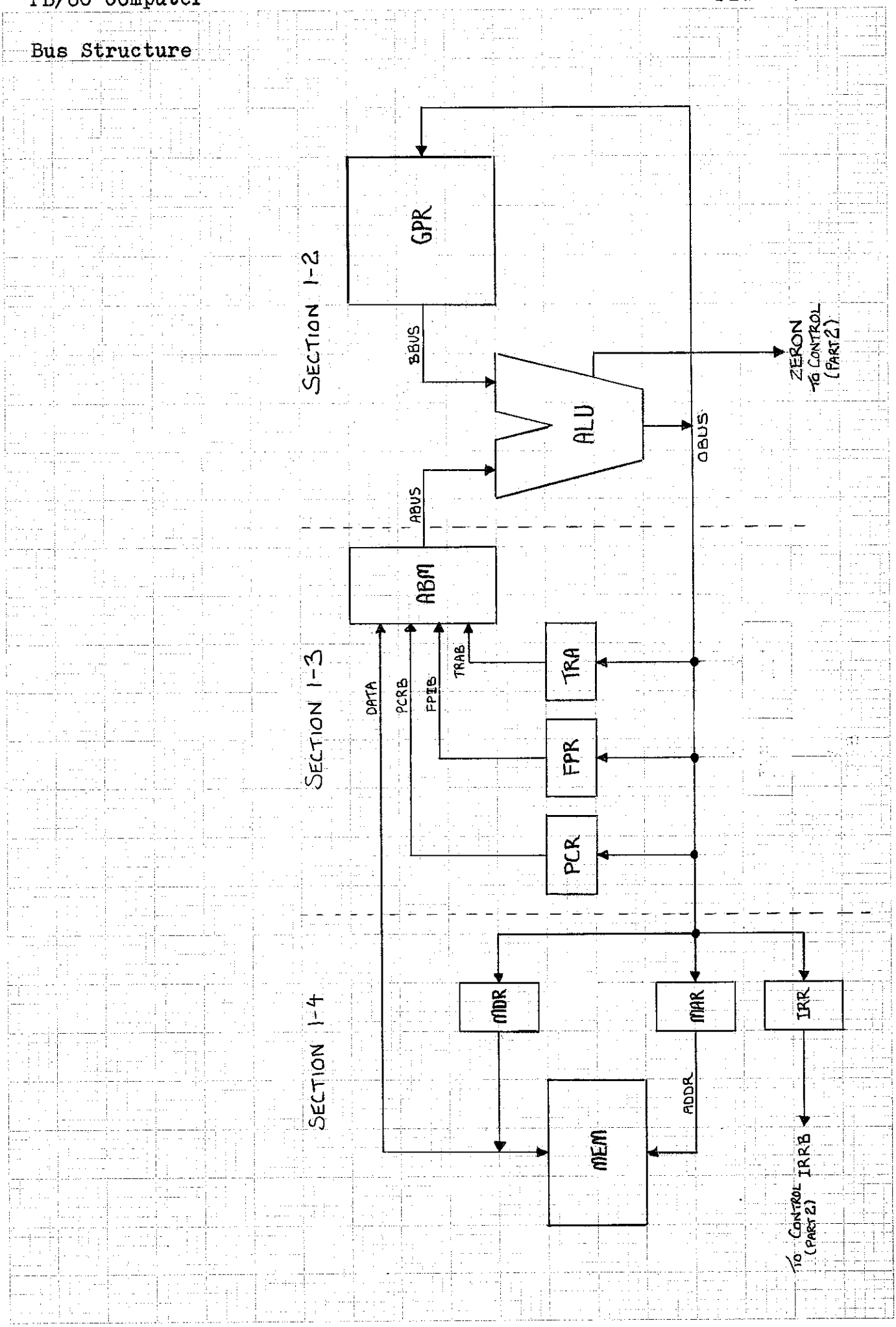
8 off resistors 5K
8 off resistors 220
8 off LED's red
8 off switches SPDT

Rev 'A' Delete - ABM-A
ABM-B
▷ NEW - TRA-RE
PCR-RE
MEM-RE
FPR-RE

PB/80 Computer

FIG 1-1

Bus Structure



ALU & GPR

Arithmetic/Logic Unit
General Purpose Registers

Buses

ABUS (Ø-7)	ALU 'A' input bus	(high true)
BBUS (Ø-7)	ALU 'B' input bus	(high true)
OBUS (Ø-7)	ALU output bus	(high true)

Control lines

GPR-GW	GPR write strobe	(low true)

GPR-RA, GPR-RB — GPR register read select

RA	RB	Select
L	L	RØ
L	H	R1
H	L	R2
H	H	R3

GPR-WA, GPR-WB — GPR register write select

WA	WB	Select
L	L	RØ
L	H	R1
H	L	R2
H	H	R3

ALU-M, ALU-C, ALU-SØ, ALU-S1, ALU-S2, ALU-S3, ALU-S/N, ALU-R/S, ALU-L/R	ALU function control	Ref. TAB 1-2
ALU-CLK	ALU output strobe	(positive edge)
ZERON	OBUS equals zero	(low true)

Devices

2 off 74181
1 off 74182
1 off 74198
2 off 74LS670
1 off 81LS96
1 off 74LS30
2 off and gates
2 off nand gates
1 off inverter

ALU function control coding

REV B

RCC bits 3 2 1 Ø	Function	ALU control lines M C S3 S2 S1 SØ S/N R/S L/R									
L L L L	F=A	L	H	L	L	L	L	L	X	X	*
L L L H	F=B	H	X	H	L	H	L	L	X	X	
L L H L	F=A+B a	L	H	L	L	L	H	L	X	X	*
L L H H	F=A-B a	L	L	L	H	H	L	L	X	X	
L H L L	F=A.B 1	H	X	H	L	H	H	L	X	X	
L H L H	F=A+B 1	H	X	H	H	H	L	L	X	X	
L H H L	F=A⊕B 1	H	X	L	H	H	L	L	X	X	
L H H H	F=AN 1	H	X	L	L	L	L	L	X	X	*
H L L L	F=A+1 a	L	L	L	L	L	L	L	X	X	*
H L L H	F=A-1 a	L	H	H	H	H	H	L	X	X	
H H L L	F=A (SR)	L	H	L	L	L	L	H	L	L	*
H H L H	F=A (SL)	L	H	L	L	L	L	H	L	H	*
H H H L	F=A (RR)	L	H	L	L	L	L	H	H	L	*
H H H H	F=A (RL)	L	H	L	L	L	L	H	H	H	*
H L H X	F=Ø	H	X	L	L	H	H	L	X	X	X

✓ ALU-S/N = RCC2.3.4

✓ ALU-R/S = RCC1

✓ ALU-L/R = RCCØ

ALU-M = (RCC2.$\overline{\text{ALU-S/N}}$)+(RCCØ.$\overline{1}$) BORING

✓ ALU-C = [(RCCØ.$\overline{1}$.$\overline{2}$.3)+(RCC$\overline{2}$.$\overline{3}$.Ø.1)]N . RESETNCE

✓ ALU-SØ = $\overline{\text{ALU-S1}}$+(RCC$\overline{\text{Ø.1}}$)+RCC3

ALU-S1 = (RCC$\overline{\text{Ø.2}}$)N + RESET

ALU-S2 = ($\overline{\text{ALU-SØ}}$+RCC3).(RCC$\overline{3.2.1}$)N

✓ ALU-S3 = $\overline{\text{RCC1}}$

✓ ZERSEL* = Zero select bits (SØ-3).

= (RCC$\overline{\text{Ø.1.2}}$)+ALU-S/N+(RCCØ.1.2)

GPR (B Source) control coding

RCB bit	Source	GPR control lines GW RB RA WB WA				
L	RØ	X	L	L	X	X
H	'r'	X	b	a	X	X
-	-	L	X	X	L	L
-	-	L	X	X	b	a

GPR (Destination) ctl. coding

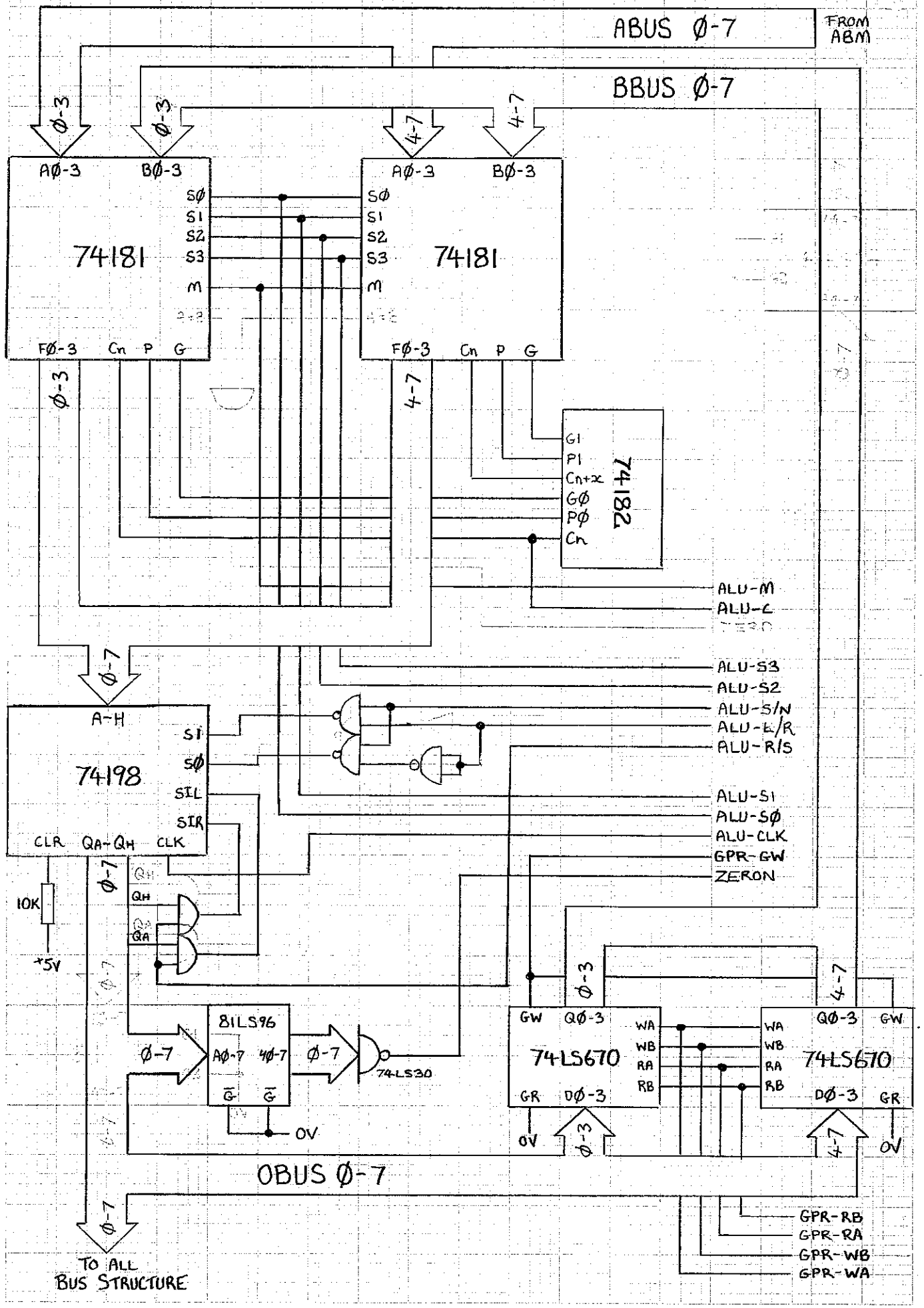
RCD bits 2 1 Ø	Destination
- - -	- -
- - -	- -
L L L	RØ
L L H	'r'

GPR-GW goes low during WRICYC

b = IRRB-1 during tn time, or FPRS-1 during fn time
a = IRRB-Ø during tn time, or FPRS-Ø during fn time

PB/80 Computer FIG 1-2

ALU & GPR Arithmetic/Logic Unit & General Purpose Registers



ABM, PCR, FPR & TRA

'A' Bus Multiplexer
Programme Counter Register
Front Panel Register
'A' bus Temporary Register

Buses

OBUS (Ø-7)	ALU output bus	(high true)
ABUS (Ø-7)	ALU 'A' input bus	(high true)
DATA (Ø-7)	Memory Data bus	(high true)
PCRB (Ø-7)	Programme Counter bus	(high true)
TRAB (Ø-7)	'A' bus Temp. Register bus	(high true)
FPIB (Ø-7)	Front Panel input bus	(high true)

Control lines

FPR-WC	FPR write clock	(positive edge)
PCR-WC	PCR write clock	(positive edge)
TRA-WC	TRA write clock	(positive edge)
ABM-A ABM-B	ABM 'A' source select	

A	B	Select
L	L	FPR
L	H	MEM
H	L	TRA
H	H	PCR

ZABUS	Zero ABUS control	(high true)

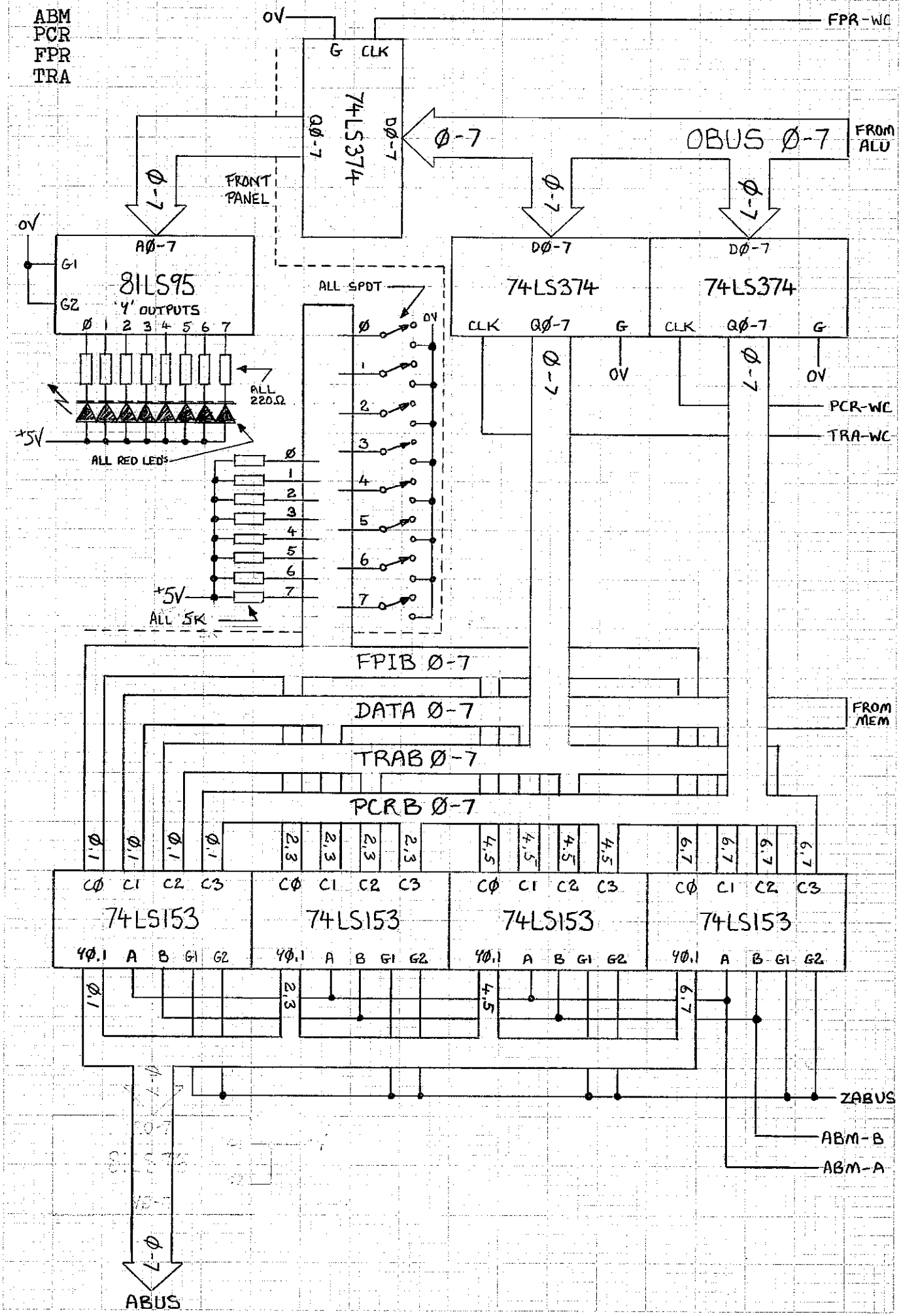
Devices

3 off 74LS374
4 off 74LS153
1 off 81LS95

8 off resistors 5K
8 off resistors 220
8 off LED's red
8 off switches SPDT

Front Panel Controls

FPO Ø thru 7	Data display LED's.
FPI Ø thru 7	Data entry switches.


ABM
PCR
FPR
TRA
0V
G CLK
74LS374
QØ-7
DØ-7
FPR-WC
Ø-7
OBUS Ø-7
FROM ALU
FRONT PANEL
AØ-7
81LS95
G1
G2
'Y' OUTPUTS
Ø 1 2 3 4 5 6 7
ALL 220Ω
+5V
ALL RED LEDS
ALL SPDT
ALL 5K
DØ-7
74LS374
CLK QØ-7 G
PCR-WC
TRA-WC
FPIB Ø-7
DATA Ø-7
TRAB Ø-7
PCRB Ø-7
FROM MEM
74LS153
CØ C1 C2 C3
YØ.1 A B G1 G2
ZABUS
ABM-B
ABM-A
ABUS

MAR, MDR, MEM & IRR

Memory Address Register
Memory Data Register
Memory (256 X 8)
Instruction Register

Buses

OBUS (Ø-7)	ALU output bus	(high true)
ADDR (Ø-7)	Memory address bus	(high true)
DATA (Ø-7)	Memory data bus (bi-directional,	high true)
IRRB (Ø-7)	Instruction register bus	(high true)

Control lines

MAR-WC	MAR write clock	(positive edge)
MDR-WC	MDR write clock	(positive edge)
IRR-WC	IRR write clock	(positive edge)
MEM-R/W	Memory read/write control high = read low = write	

Devices

3 off 74LS374
2 off 2112

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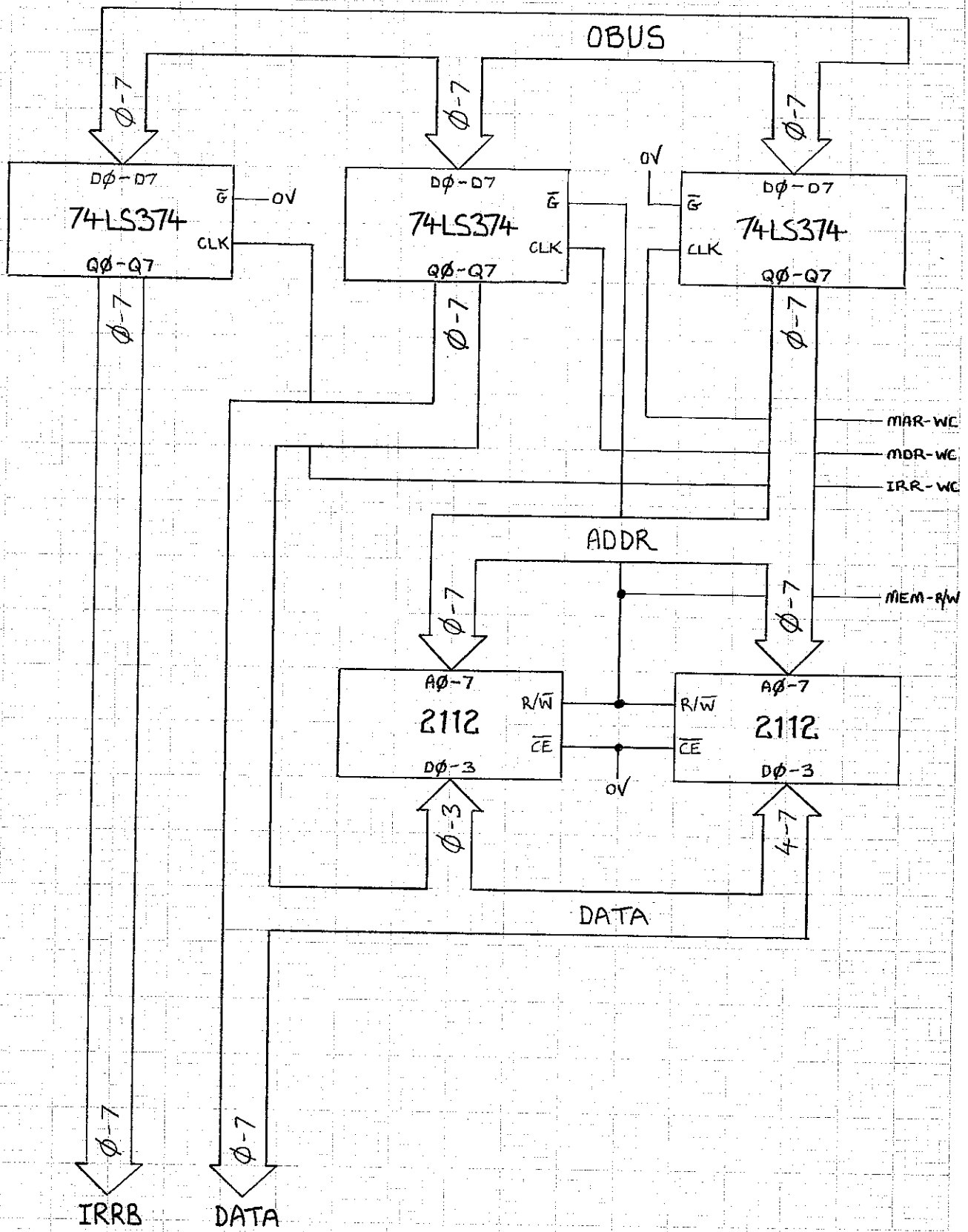
FIG 1-4

MAR Memory address register
MDR Memory data register
MEM Memory (256 X 8)
IRR Instruction register



RCA	ROM 'A' Source control decoder
RCB	ROM 'B' Source control decoder
RCC	ROM ALU function control decoder
RCD	ROM Destination control decoder
RCE	ROM Instruction end control decoder

Control lines in

RCA-Ø,1	'A' Source code from ROM	(Ref: TAB 2-2)
RCB-Ø	'B' Source code from ROM	
RCC-Ø,3	ALU Function code from ROM	
RCD-Ø,2	Destination code from ROM	
RCE-Ø,1	Instruction end code from ROM	
REGC-Ø,1	Register select code from RAM	(high true)
ZERON	OBUS zero detect signal	(low true)
HALTN	Halt state signal	(low true)
WRICYC	Write timing cycle signal	(high true)
INCCYCN	Increment timing cycle signal	(low true)

Control lines out

ABM-A ABM-B	'A' Source control select	(high true)
GPR-RA GPR-RB	'B' Source register select	(high true)
ALU-R/S ALU-L/R ALU-S/N ALU-M ALU-C ALU-SØ ALU-S1 ALU-S2 ALU-S3	ALU Function control	
GPR-WA GPR-WB	GPR Destination select	(high true)
GPR-GW FPR-WC TRA-WC MDR-WC MAR-WC PCR-WC IRR-WC	Destination write clocks	(positive edge)
MEM-R/W	Memory write clock	(low true)
INSEND	End instruction time	(high true)
INCRTA	Increment instruction (tn) time	(high true)

Internal signals

ZERSELN	Zero select bits SØ,3 (RCC)	(low true)
DESTRØN	Destination RØ (RCD)	(low true)
FPDREQ	Front panel data request (RCA/E)	(high true)

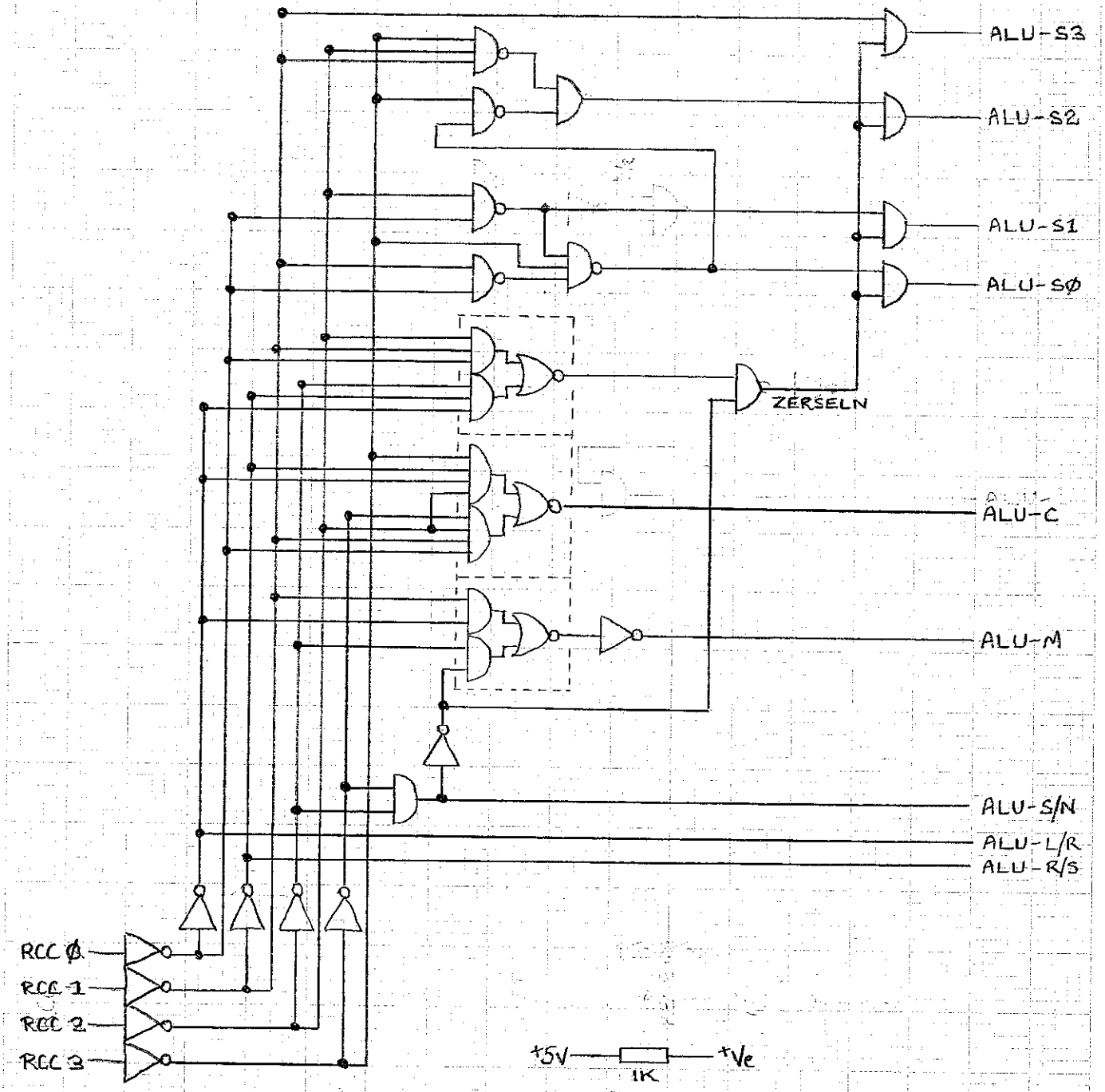
Devices

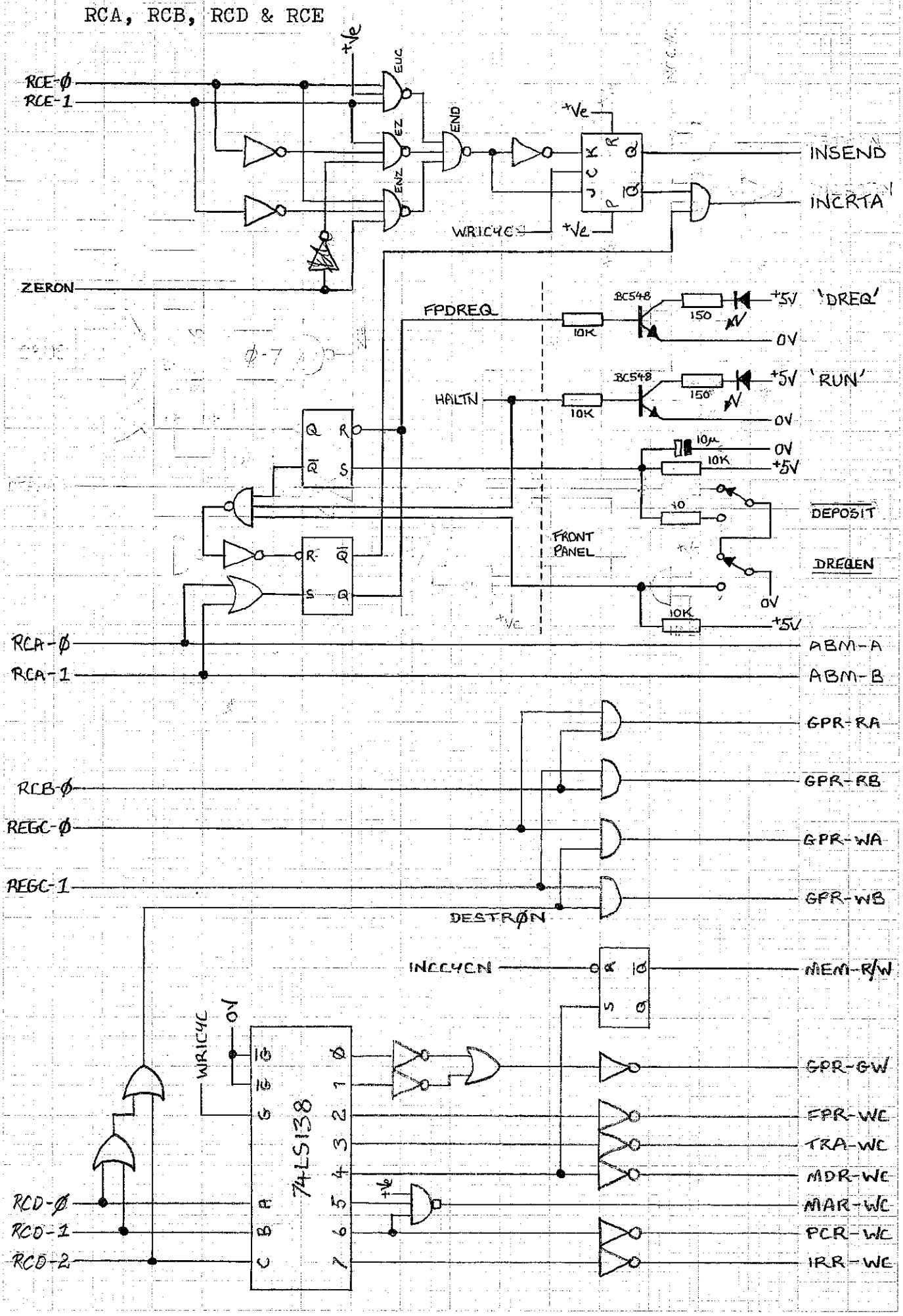
23	off inverters	4 off	74LSØ4
12	off AND2	3 off	74LSØ8
3	off NAND2	1 off	74LSØØ
8	off NAND3	3 off	74LS1Ø
4	off OR2	1 off	74LS32
1	off switch SPDT		
1	off AND2OR2INV		
1	off AND3OR2INV	1 off	74LS51
1	off AND4OR2INV	1 off	74LS55
4	off JKFF (net)	2 off	74LS76
1	off switch SPDT momentary		
1	off 3 to 8 decoder	1 off	74LS138
1	off resistor 1K		
4	off resistors 10K		
2	off resistors 150		
1	off resistor 10		
1	off capacitor 10uf tant.		
2	off transistors BC548		
2	off LED's red.		

Front panel controls

DREQ	Data request from FPR LED.
RUN	'Run' state indicator LED.
DEPOSIT	FPR data deposit switch.
DREQEN	DREQ wait enable/disable.

RCC ROM ALU function control decoder.
(Ref: TAB 1-2)




RCA, RCB, RCD & RCE
RCE-Ø
RCE-1
+Ve
EUC
EZ
ENZ
END
INSEND
INCRTA
WRICYC
ZERON
FPDREQ
10K
BC548
150
+5V
'DREQ'
0V
HALTN
'RUN'
10µ
DEPOSIT
FRONT PANEL
DREQEN
RCA-Ø
RCA-1
ABM-A
ABM-B
RCB-Ø
REGC-Ø
REGC-1
GPR-RA
GPR-RB
GPR-WA
GPR-WB
DESTRØN
INCCYCN
MEM-R/W
74LS138
GPR-GW
FPR-WC
TRA-WC
MDR-WC
MAR-WC
PCR-WC
IRR-WC
RCD-Ø
RCD-1
RCD-2

ROM, RAM & FPC

Sequence control ROM, ROM address MUX and Front panel control.

Control lines in

IRRB-Ø,7	Instruction register bus	(high true)
RAM-A,B	ROM address source select	(Ref. TAB 2-3)
ROMA-Ø,1	ROM time address	(Ref. TAB 2-3)
INCCYC	Increment timing cycle signal	(high true)
fØ	fØ time signal	(high true)
f1	f1 time signal	(high true)

Control lines out

RCA-Ø,1	'A' source code	
RCB-Ø	'B' source code	
RCC-Ø,3	ALU function code	(Ref. TAB 2-2)
RCD-Ø,2	Destination code	
RCE-Ø,1	Instruction end code	
REGC-Ø,1	Register select code	(high true)
HALTIN	HALT instruction detect signal	(high true)
ZABUS	Zero 'A' bus (reset detect)	(high true)

Internal signals

RSTINT	Reset interupt	(high true)
FPCB-Ø,2	Front panel control bus	(Ref. TAB 2-3)
FPRS-Ø,1	Front panel register select	(high true)
ROMA-2,7	ROM instruction/macro address	(Ref. TAB 2-3) (Appendix A)

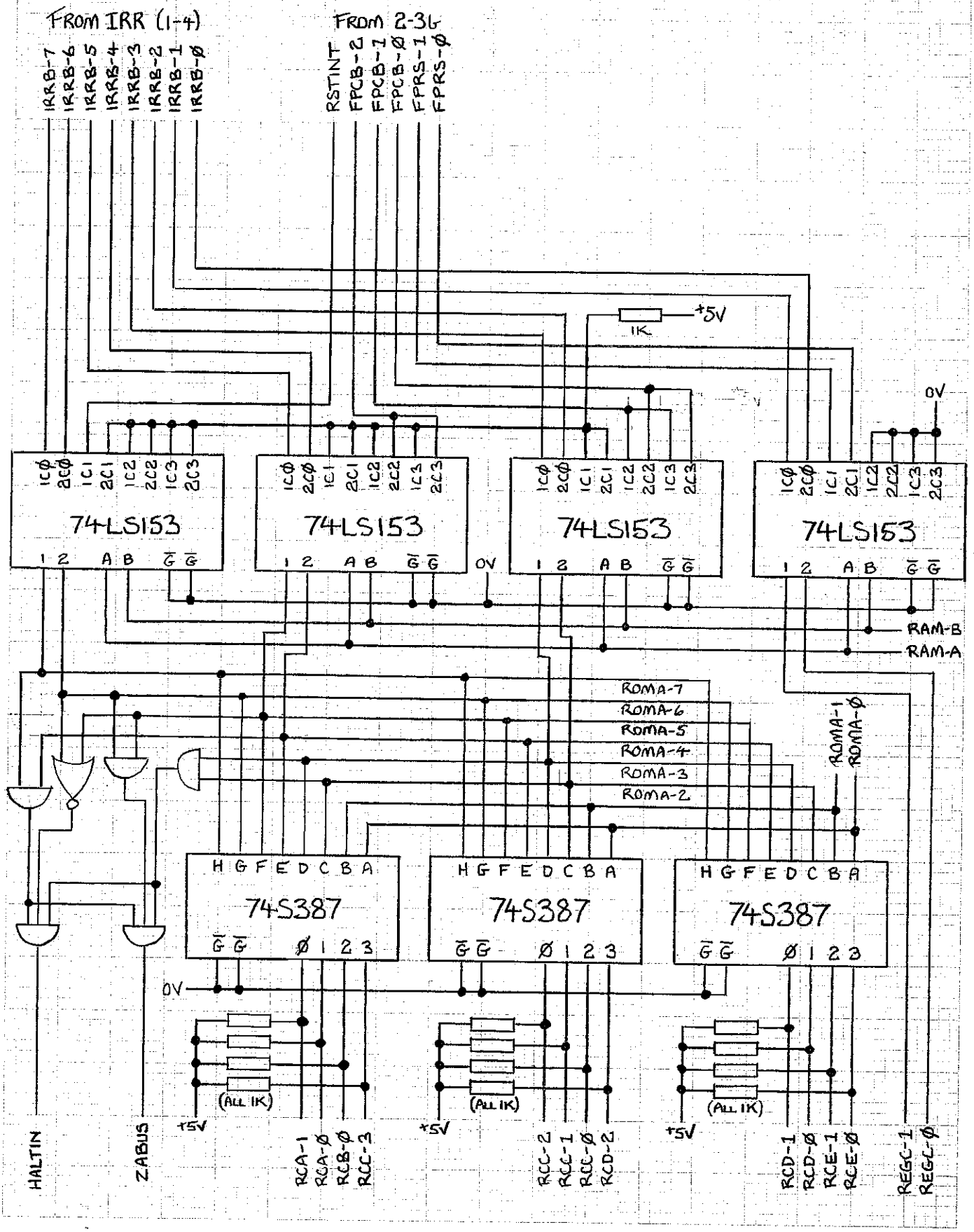
Devices

1 off 74LS148
2 off 74LS76
1 off 74LS174
4 off 74LS153
3 off 74S387
1 off 74LSØ2
1 off 74LSØ8
1 off 74LS11
17 off resistors 1K
8 off resistors 10K
7 off resistors 10
7 off capacitors 10uf tant.
2 off switches SPDT
5 off switches SPDT momentary
1 off switch DPDT

Front panel controls

REG/MEM DIS/LOA	Register/memory-display/load select.
DIS-PCR	Display PCR switch
INC-PCR	Increment PCR switch
LOA-PCR	Load PCR switch
RESET	Reset switch (reset PCR)
REG-Ø,1	Register select switches

RAM ROM Address Multiplexer
ROM ROM sequence controller



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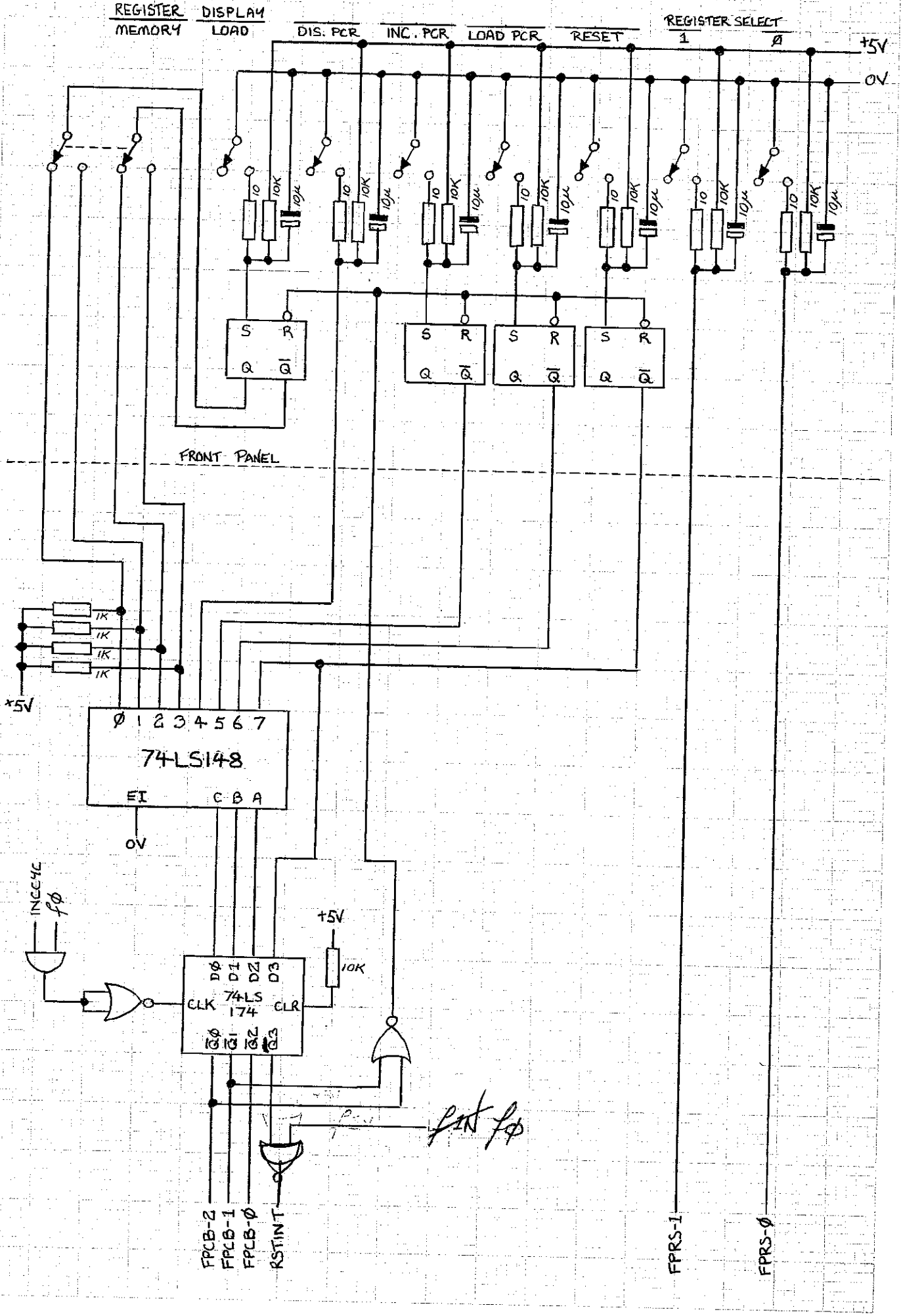
FPC Front Panel Control

FIG 2-3b



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Front Panel (Scale 2:3)

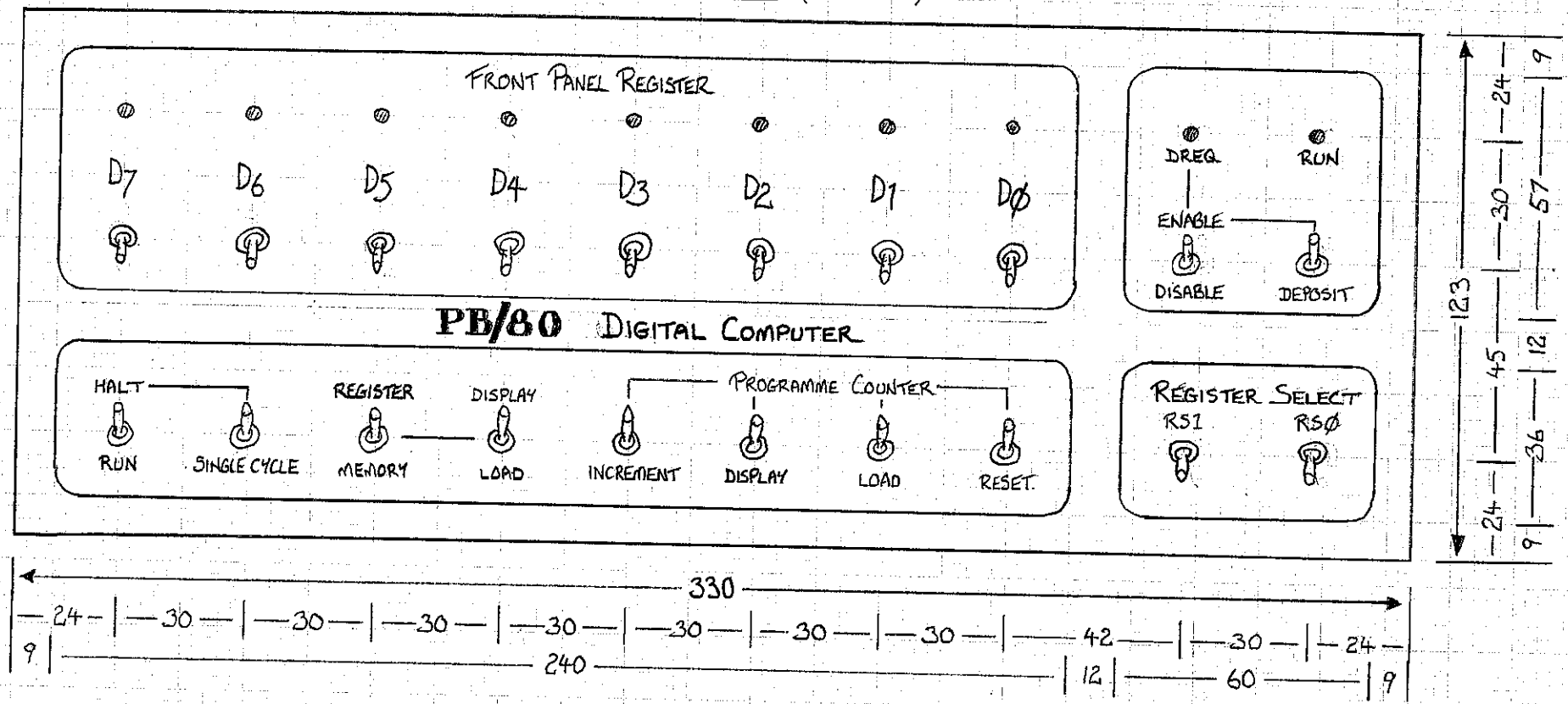
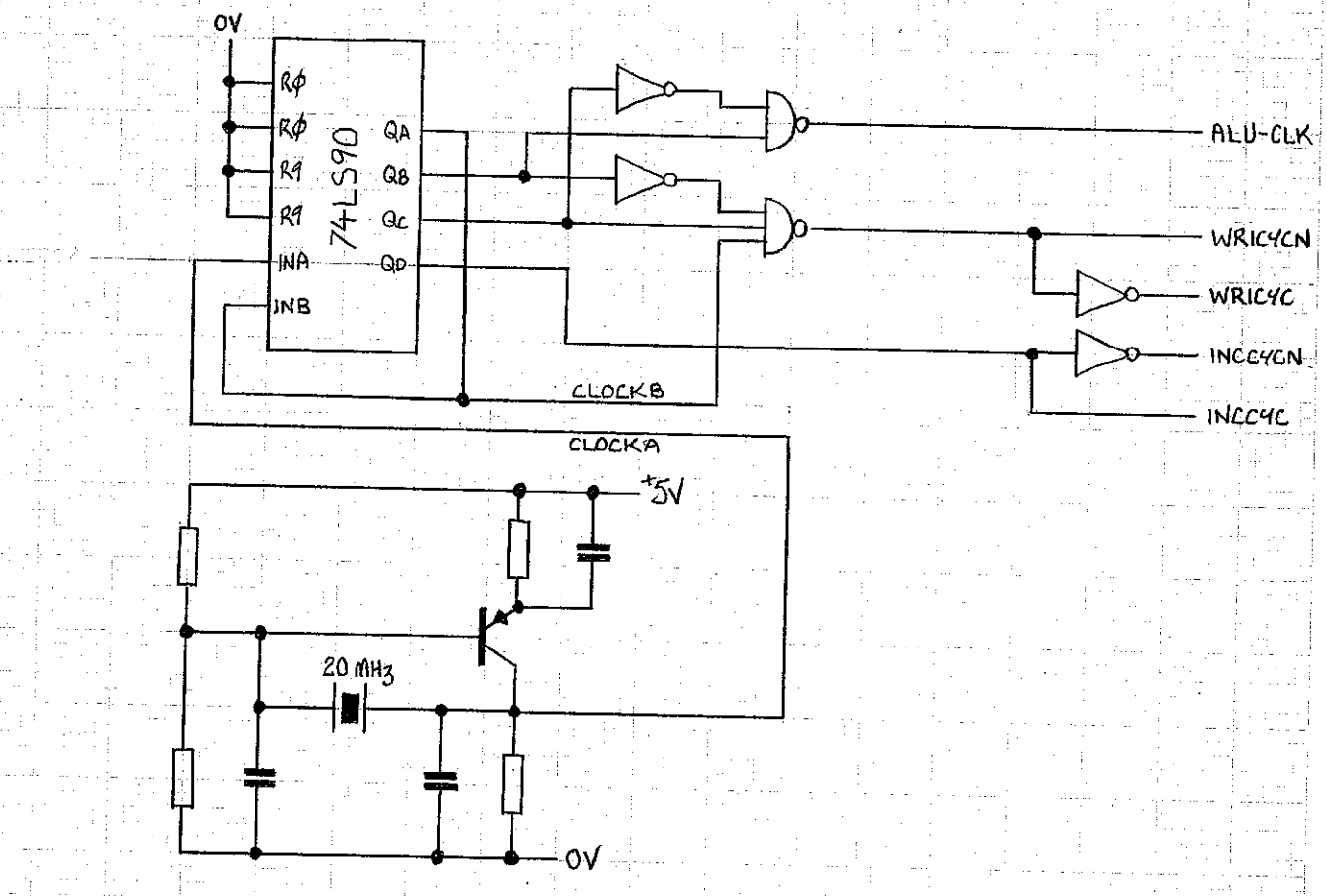


FIG 2-4a

CLK Clock generator



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